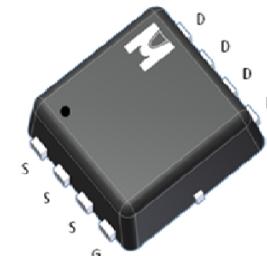
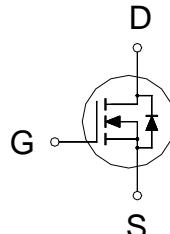


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	30V
$R_{DS(on)}(\text{MAX.})$	$3.0\text{m}\Omega$
I_D	37A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	37	A
	$T_C = 100^\circ\text{C}$		25	
Pulsed Drain Current ¹		I_{DM}	148	
Avalanche Current		I_{AS}	37	
Avalanche Energy	$L = 0.1\text{mH}, I_D=37\text{A}, R_G=25\Omega$	E_{AS}	68.4	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	34.2	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	21	W
	$T_C = 100^\circ\text{C}$		8.3	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 100^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$	6	50	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	37			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 18A$		2.5	3.0	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 14A$		3.0	4.0	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 18A$		25		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		2979		pF
Output Capacitance	C_{oss}			381		
Reverse Transfer Capacitance	C_{rss}			224		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		1.6		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 18A$		44.6		nC
	$Q_g(V_{GS}=4.5V)$			21.2		
Gate-Source Charge ^{1,2}	Q_{gs}			8.3		
Gate-Drain Charge ^{1,2}	Q_{gd}			6.5		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		15		nS
Rise Time ^{1,2}	t_r			10		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			50		
Fall Time ^{1,2}	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, dI_F/dt = 100\text{A} / \mu\text{s}$			37	A
Pulsed Current ³	I_{SM}				148	
Forward Voltage ¹	V_{SD}		$I_F = I_S, V_{GS} = 0V$		1.3	V
Reverse Recovery Time	t_{rr}			32		nS
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			200		A
Reverse Recovery Charge	Q_{rr}			12		nC

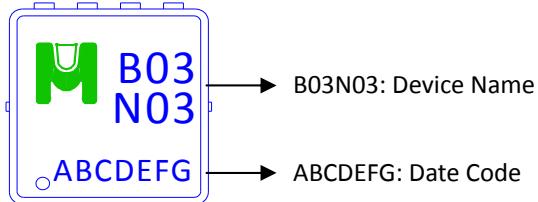
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

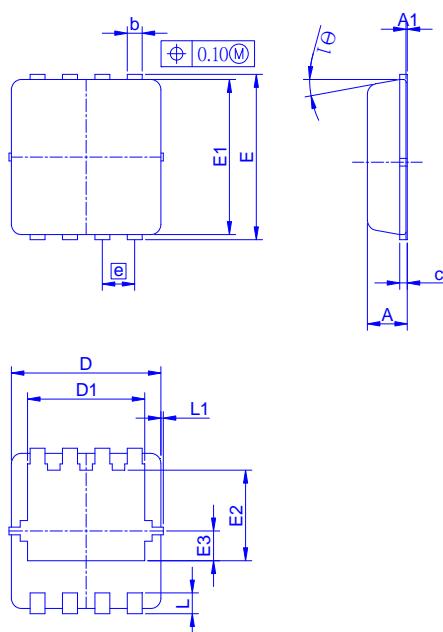
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB03N03V for EDFN 3 x 3

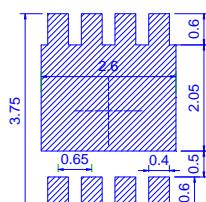


Outline Drawing



Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads



TYPICAL CHARACTERISTICS

